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**Jameco Part Number 39773**

## Features

- **Fast Read Access Time - 45 ns**
- **Low-Power CMOS Operation**
  - **100 µA max. Standby**
  - **20 mA max. Active at 5 MHz**
- **JEDEC Standard Packages**
  - **28-Lead 600-mil PDIP**
  - **32-Lead PLCC**
  - **28-Lead TSOP and SOIC**
- **5V ± 10% Supply**
- **High-Reliability CMOS Technology**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid™ Programming Algorithm - 100 µs/byte (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial, Industrial and Automotive Temperature Ranges**

# 512K (64K x 8) OTP EPROM

# AT27C512R

## Description

The AT27C512R is a low-power, high-performance 524,288-bit one-time programmable read only memory (OTP EPROM) organized 64K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

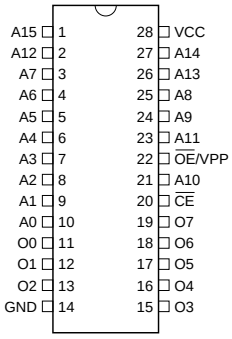
Atmel's scaled CMOS technology provides high-speed, lower active power consumption, and significantly faster programming. Power consumption is typically only 8 mA in Active Mode and less than 10 µA in Standby.

*(continued)*

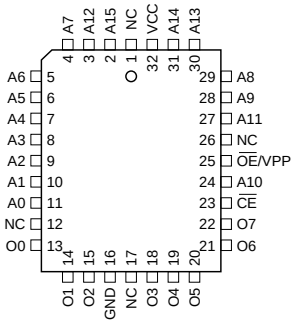
## Pin Configurations

| Pin Name | Function |
|---|---|
| A0 to A15 | Addresses |
| O0 - O7 | Outputs |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$/VPP | Output Enable/VPP |
| NC | No Connect |

PDIP, SOIC Top View

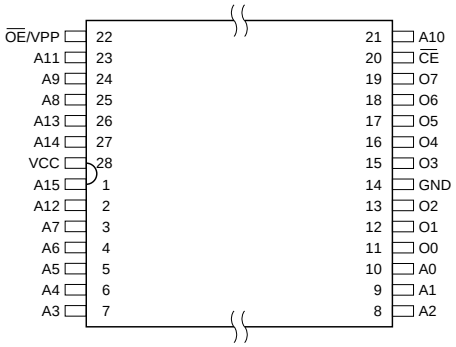



PLCC Top View




TSOP Top View

**Type 1**




Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Rev. 0015I–07/98

The AT27C512R is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, SOIC, and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

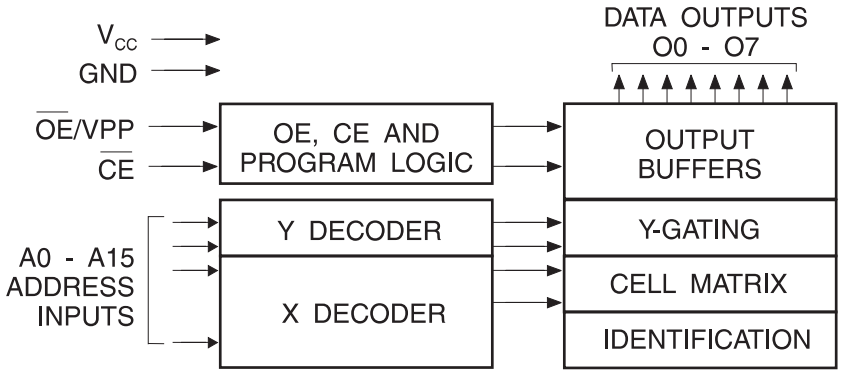
With 64K byte storage capability, the AT27C512R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C512R has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

## System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the $V_{CC}$ and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the $V_{CC}$ and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## Block Diagram




## Absolute Maximum Ratings*

| | |
|---|---|
| Temperature Under Bias | -55°C to + 125°C |
| Storage Temperature | -65°C to + 150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to + 7.0V(1) |
| Voltage on A9 with Respect to Ground | -2.0V to + 14.0V(1) |
| $V_{PP}$ Supply Voltage with Respect to Ground | -2.0V to + 14.0V(1) |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC}$ + 0.75V dc which may overshoot to +7.0 volts for pulses of less than 20 ns.

## Operating Modes

| Mode\Pin | $\overline{CE}$ | $\overline{OE}/V_{PP}$ | Ai | Outputs |
|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | Ai | $D_{OUT}$ |
| Output Disable | $V_{IL}$ | $V_{IH}$ | X(1) | High Z |
| Standby | $V_{IH}$ | X(1) | X | High Z |
| Rapid Program(2) | $V_{IL}$ | $V_{PP}$ | Ai | $D_{IN}$ |
| PGM Inhibit | $V_{IH}$ | $V_{PP}$ | X(1) | High Z |
| Product Identification(4) | $V_{IL}$ | $V_{IL}$ | A9 = $V_H$(3)<br>A0 = $V_{IH}$ or $V_{IL}$<br>A1 - A15 = $V_{IL}$ | Identification Code |

Notes:
1. X can be $V_{IL}$ or $V_{IH}$.
2. Refer to Programming Characteristics.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low ($V_{IL}$), except A9 which is set to $V_H$ and A0 which is toggled low ($V_{IL}$) to select the Manufacturer's Identification byte and high ($V_{IH}$) to select the Device Code byte.

## DC and AC Operating Conditions for Read Operation

| | | AT27C512R | | | | | |
|---|---|---|---|---|---|---|---|
| | | -45 | -55 | -70 | -90 | -12 | -15 |
| Operating Temp.(Case) | Com. | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C | 0°C - 70°C |
| | Ind. | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C | -40°C - 85°C |
| | Auto. | | | -40°C - 125°C | -40°C - 125°C | -40°C - 125°C | -40°C - 125°C |
| $V_{CC}$ Supply | | 5V ± 10% | 5V ± 10% | 5V ± 10% | 5V ± 10% | 5V ± 10% | 5V ± 10% |

## DC and Operating Characteristics for Read Operation

| Symbol | Parameter | Condition | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ | Com., Ind, | | ±1 | µA |
| | | | Auto. | | ±5 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{CC}$ | Com., Ind, | | ±5 | µA |
| | | | Auto. | | ±10 | µA |
| $I_{SB}$ | $V_{CC}$(1) Standby Current | $I_{SB1}$ (CMOS), $\overline{CE}$ = $V_{CC}$ ± 0.3V | | | 100 | µA |
| | | $I_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V | | | 1 | mA |
| $I_{CC}$ | $V_{CC}$ Active Current | f = 5 MHz, $I_{OUT}$ = 0 mA, $\overline{CE}$ = $V_{IL}$ | | | 20 | mA |
| $V_{IL}$ | Input Low Voltage | | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -400 µA | | 2.4 | | V |

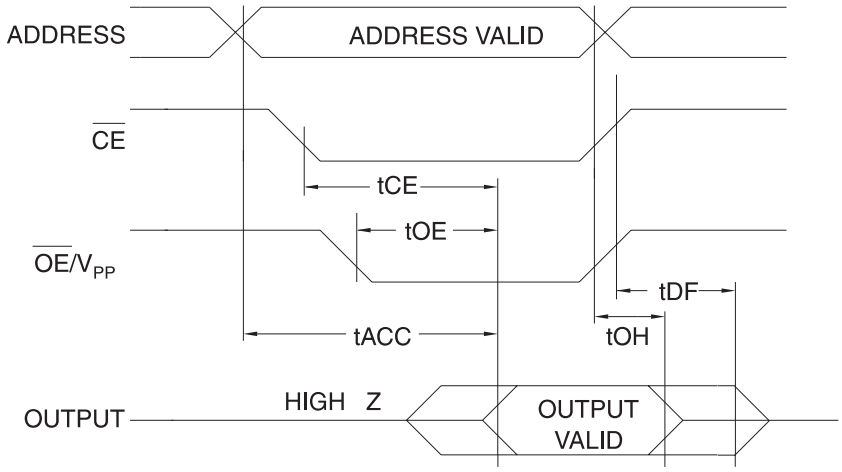
Notes: 1. $V_{CC}$ must be applied simultaneously with or before $\overline{OE}/V_{PP}$ and removed simultaneously with or after $\overline{OE}/V_{PP}$.

## AC Characteristics for Read Operation

| | | | AT27C512R | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -45 | | -55 | | -70 | | -90 | | -12 | | -15 | | |
| Symbol | Parameter | Condition | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Units |
| $t_{ACC}$(3) | Address to Output Delay | $\overline{CE}$= $\overline{OE}/V_{PP}$ = $V_{IL}$ | | 45 | | 55 | | 70 | | 90 | | 120 | | 150 | ns |
| $t_{CE}$(2) | $\overline{CE}$ to Output Delay | $\overline{OE}/V_{PP}$ = $V_{IL}$ | | 45 | | 55 | | 70 | | 90 | | 120 | | 150 | ns |
| $t_{OE}$(2)(3) | $\overline{OE}/V_{PP}$ to Output Delay | $\overline{CE}$ = $V_{IL}$ | | 20 | | 25 | | 30 | | 35 | | 35 | | 40 | ns |
| $t_{DF}$(4)(5) | $\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, whichever occurred first | | | 20 | | 20 | | 25 | | 25 | | 30 | | 35 | ns |
| $t_{OH}$ | Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occurred first | | 7 | | 7 | | 7 | | 0 | | 0 | | 0 | | ns |

Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

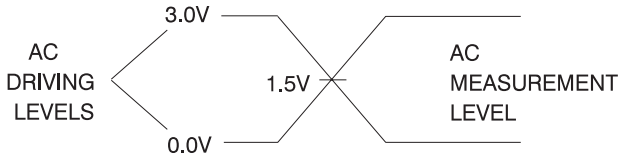
## AC Waveforms for Read Operation(1)




Notes:
1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are $V_{IL}$ = 0.0V and $V_{IH}$ = 3.0V. Timing measurement reference levels for all other speed grades are $V_{OL}$ = 0.8V and $V_{OH}$ = 2.0V. Input AC drive levels are $V_{IL}$ = 0.45V and $V_{IH}$ = 2.4V.
2. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE}$ - $t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC}$ - $t_{OE}$ after the address is valid without impact on $t_{ACC}$.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

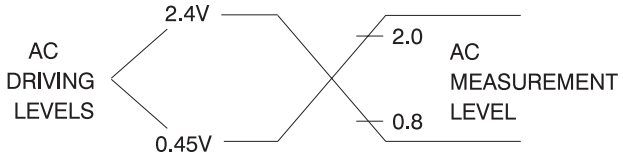
## Input Test Waveforms and Measurement Levels

For -45 and -55 devices only:



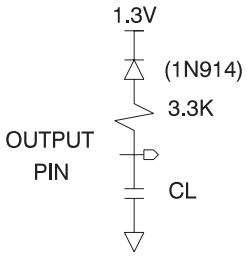

$t_R$, $t_F$ < 5 ns (10% to 90%)

For -70, -90, -12, -15, and -20 devices:




$t_R$, $t_F$ < 20 ns (10% to 90%)

## Output Test Load




Note: $C_L$ = 100 pF including jig capacitance, except for the -45 and -55 devices, where $C_L$ = 30 pF.

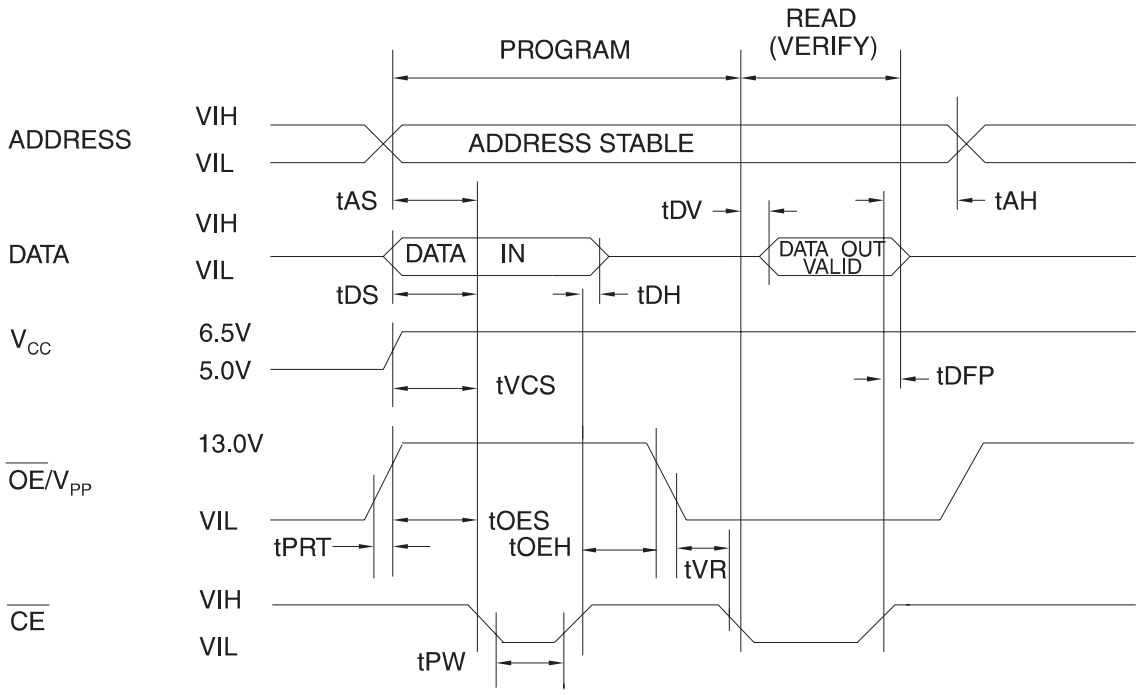
## Pin Capacitance

(f = 1 MHz T = 25°C)(1)

| | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 6 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## Programming Waveforms[1]




Notes: 1. The Input Timing Reference is 0.8V for $V_{IL}$ and 2.0V for $V_{IH}$.

2. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer.

## DC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

| Symbol | Parameter | Test Conditions | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{IL}, V_{IH}$ | | ±10 | µA |
| $V_{IL}$ | Input Low Level | | -0.6 | 0.8 | V |
| $V_{IH}$ | Input High Level | | 2.0 | $V_{CC}$ + 1 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -400 µA | 2.4 | | V |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program and Verify) | | | 25 | mA |
| $I_{PP2}$ | $\overline{OE}/V_{PP}$ Current | $\overline{CE} = V_{IL}$ | | 25 | mA |
| $V_{ID}$ | A9 Product Identification Voltage | | 11.5 | 12.5 | V |

## AC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25V$, $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$

| Symbol | Parameter | Test Conditions[1] | Limits | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $t_{AS}$ | Address Setup Time | Input Rise and Fall Times (10% to 90%) 20ns<br>Input Pulse Levels 0.45V to 2.4V<br>Input Timing Reference Level 0.8V to 2.0V<br>Output Timing Reference Level 0.8V to 2.0V | 2 | | µs |
| $t_{OES}$ | $\overline{OE}/V_{PP}$ Setup Time | | 2 | | µs |
| $t_{OEH}$ | $\overline{OE}/V_{PP}$ Hold Time | | 2 | | µs |
| $t_{DS}$ | Data Setup Time | | 2 | | µs |
| $t_{AH}$ | Address Hold Time | | 0 | | µs |
| $t_{DH}$ | Data Hold Time | | 2 | | µs |
| $t_{DFP}$ | $\overline{CE}$ High to Output Float Delay[2] | | 0 | 130 | ns |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | µs |
| $t_{PW}$ | $\overline{CE}$ Program Pulse Width[3] | | 95 | 105 | µs |
| $t_{DV}$ | Data Valid from $\overline{CE}$[2] | | | 1 | µs |
| $t_{VR}$ | $\overline{OE}/V_{PP}$ Recovery Time | | 2 | | µs |
| $t_{PRT}$ | $\overline{OE}/V_{PP}$ Pulse Rise Time During Programming | | 50 | | ns |

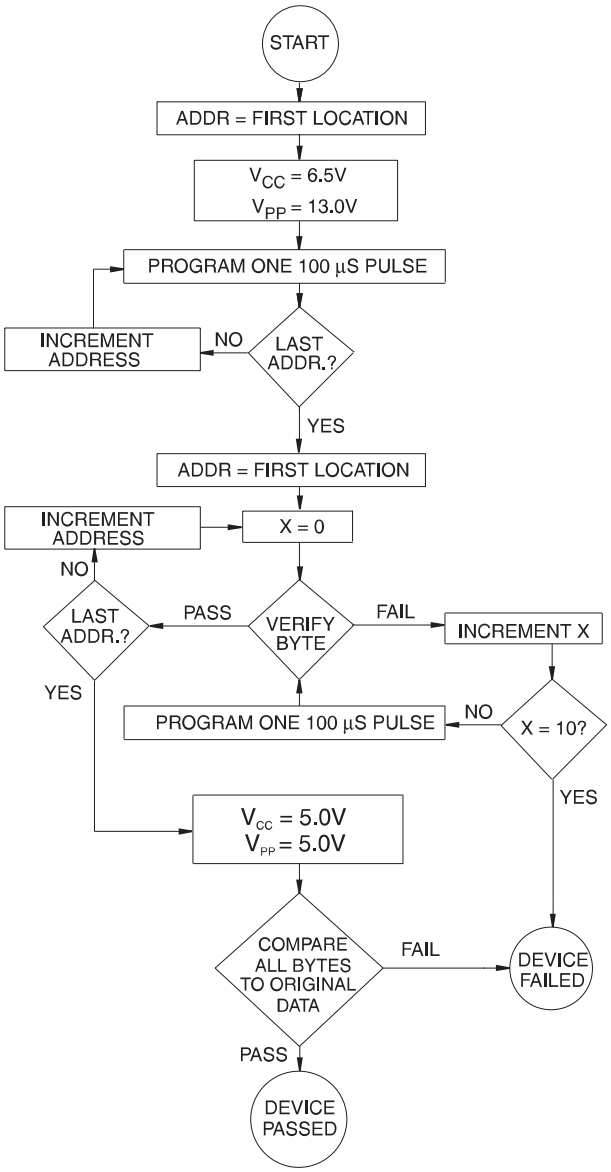
Notes:
1. $V_{CC}$ must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

## Atmel's 27C512R Integrated Product Identification Code

| Codes | Pins | | | | | | | | | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| | A0 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 | |
| Manufacturer | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E |
| Device Type | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D |

## Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. $V_{CC}$ is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to $V_{IL}$ and $V_{CC}$ to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



## Ordering Information

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 45 | 20 | 0.1 | AT27C512R-45JC<br>AT27C512R-45PC<br>AT27C512R-45RC<br>AT27C512R-45TC | 32J<br>28P6<br>28R<br>28T | Commercial<br>(0°C to 70°C) |
| | 20 | 0.1 | AT27C512R-45JI<br>AT27C512R-45PI<br>AT27C512R-45RI<br>AT27C512R-45TI | 32J<br>28P6<br>28R<br>28T | Industrial<br>(-40°C to 85°C) |
| 55 | 20 | 0.1 | AT27C512R-55JC<br>AT27C512R-55PC<br>AT27C512R-55RC<br>AT27C512R-55TC | 32J<br>28P6<br>28R<br>28T | Commercial<br>(0°C to 70°C) |
| | 20 | 0.1 | AT27C512R-55JI<br>AT27C512R-55PI<br>AT27C512R-55RI<br>AT27C512R-55TI | 32J<br>28P6<br>28R<br>28T | Industrial<br>(-40°C to 85°C) |
| 70 | 20 | 0.1 | AT27C512R-70JC<br>AT27C512R-70PC<br>AT27C512R-70RC<br>AT27C512R-70TC | 32J<br>28P6<br>28R<br>28T | Commercial<br>(0°C to 70°C) |
| | 20 | 0.1 | AT27C512R-70JI<br>AT27C512R-70PI<br>AT27C512R-70RI<br>AT27C512R-70TI | 32J<br>28P6<br>28R<br>28T | Industrial<br>(-40°C to 85°C) |
| | 20 | 0.1 | AT27C512R-70JA<br>AT27C512R-70PA<br>AT27C512R-70RA | 32J<br>28P6<br>28R | Automotive<br>(-40°C to 125°C) |

*(continued)*

| Package Type | |
|---|---|
| **32J** | 32-Lead, Plastic J-Leaded Chip Carrier (PLCC) |
| **28P6** | 28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **28R** | 28-Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC) |
| **28T** | 28-Lead, Thin Small Outline Package (TSOP) |

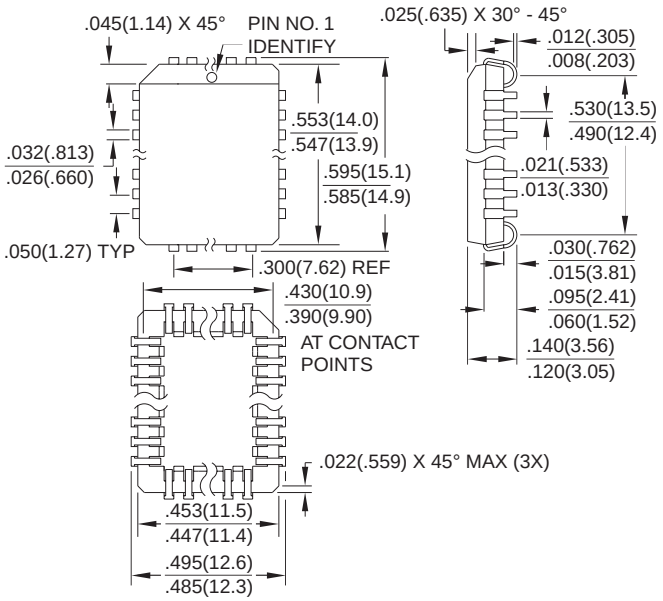
## Ordering Information (Continued)

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 90 | 20 | 0.1 | AT27C512R-90JC<br>AT27C512R-90PC<br>AT27C512R-90RC<br>AT27C512R-90TC | 32J<br>28P6<br>28R<br>28T | Commercial<br>(0°C to 70°C) |
| | 20 | 0.1 | AT27C512R-90JI<br>AT27C512R-90PI<br>AT27C512R-90RI<br>AT27C512R-90TI | 32J<br>28P6<br>28R<br>28T | Industrial<br>(-40°C to 85°C) |
| | 20 | 0.1 | AT27C512R-90JA<br>AT27C512R-90PA<br>AT27C512R-90RA | 32J<br>28P6<br>28R | Automotive<br>(-40°C to 125°C) |
| 120 | 20 | 0.1 | AT27C512R-12JC<br>AT27C512R-12PC<br>AT27C512R-12RC<br>AT27C512R-12TC | 32J<br>28P6<br>28R<br>28T | Commercial<br>(0°C to 70°C) |
| | 20 | 0.1 | AT27C512R-12JI<br>AT27C512R-12PI<br>AT27C512R-12RI<br>AT27C512R-12TI | 32J<br>28P6<br>28R<br>28T | Industrial<br>(-40°C to 85°C) |
| | 20 | 0.1 | AT27C512R-12JA<br>AT27C512R-12PA<br>AT27C512R-12RA | 32J<br>28P6<br>28R | Automotive<br>(-40°C to 125°C) |
| 150 | 20 | 0.1 | AT27C512R-15JC<br>AT27C512R-15PC<br>AT27C512R-15RC<br>AT27C512R-15TC | 32J<br>28P6<br>28R<br>28T | Commercial<br>(0°C to 70°C) |
| | 20 | 0.1 | AT27C512R-15JI<br>AT27C512R-15PI<br>AT27C512R-15RI<br>AT27C512R-15TI | 32J<br>28P6<br>28R<br>28T | Industrial<br>(-40°C to 85°C) |
| | 20 | 0.1 | AT27C512R-15JA<br>AT27C512R-15PA<br>AT27C512R-15RA | 32J<br>28P6<br>28R | Automotive<br>(-40°C to 125°C) |

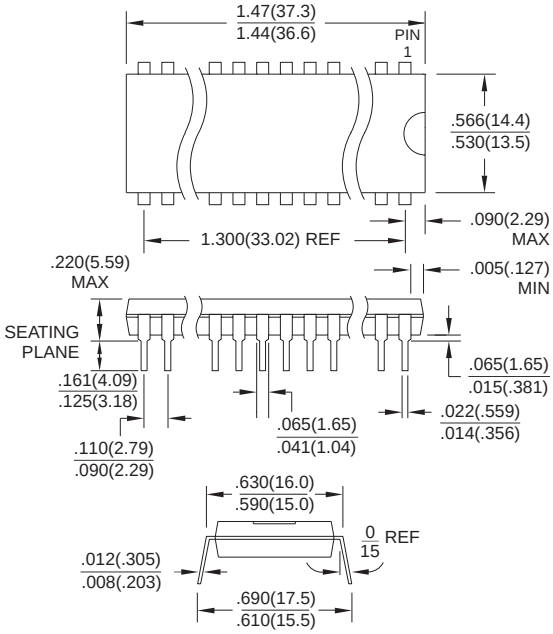
| Package Type | |
|---|---|
| **32J** | 32-Lead, Plastic J-Leaded Chip Carrier (PLCC) |
| **28P6** | 28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **28R** | 28-Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC) |
| **28T** | 28-Lead, Thin Small Outline Package (TSOP) |

## Packaging Information

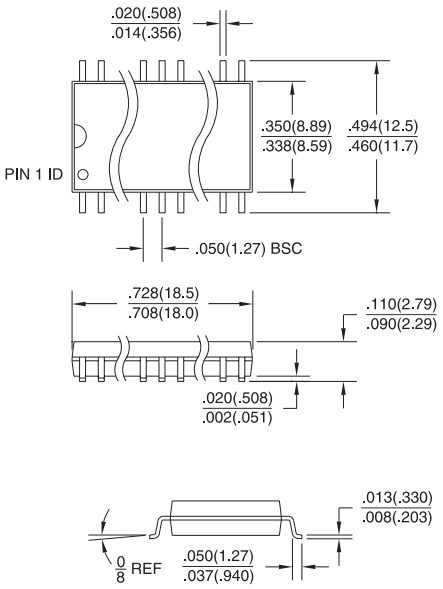
**32J**, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE



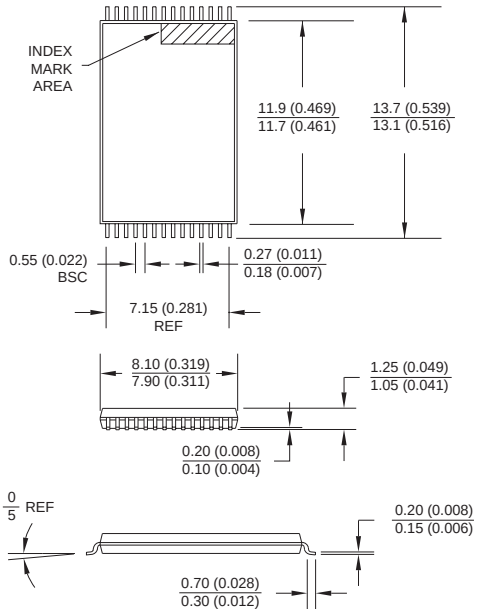

**28P6**, 28-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AB




**28R**, 28-Lead, 0.330" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)




**28T**, 28-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*




*Controlling dimension: millimeters

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